AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1. – 49. (Cancelled)

50. (Previously Presented) A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming a bonding pad and an extraction electrode each comprised of an uppermost layer wiring in a product circuit region;

(b) forming a protection film on an upper layer of said uppermost layer wiring; and

(c) partially exposing a surface of said bonding pad by removing a predetermined part of said protection film,

wherein said uppermost layer wiring is formed by depositing a conductive body and then patterning by a lithography method,

a plurality of logic circuits provided with said extraction electrode are formed in said product circuit region, and

after partially exposing the surface of said extraction electrode by removing said protection film on said extraction electrode, a probe having a tip radius of curvature of about 0.05 μm to 0.8 μm is contacted to said extraction electrode, and then logic values of said logic circuits are evaluated.

51. (Previously Presented) The method of manufacturing a semiconductor device according to claim 50;

wherein said protection film on said extraction electrode is removed by a focused ion beam method or a selective etching method.

52. (Previously Presented) The method of manufacturing a semiconductor device according to claim 50;

wherein said logic circuit comprises n input terminals and m output terminals, and n + m + 3 probes are contacted to said extraction electrodes to evaluate a logic value of said logic circuit.

53. (Previously Presented) The method of manufacturing a semiconductor device according to claim 52,

wherein one of said probes is a probe for contact confirmation.

54. (Previously Presented) The method of manufacturing a semiconductor device according to claim 50,

wherein said probe contains tungsten as a main component.

55. (Previously Presented) The method of manufacturing a semiconductor device according to claim 50,

wherein said logic circuits are TEG elements.

56. – 60. (Canceled)